

1. General Description

This EPROM-Based 8bit micro-controller uses a fully static CMOS technology process to achieve higher speed and smaller size with the low power consumption and high noise immunity. On chip memory includes 1K words of ROM, and 36 bytes of static RAM.

2. Features

The followings are some of the features on the hardware and software :

- ◆ Fully COMS static design
- ◆ 8-bit data bus
- ◆ On chip EPROM size : 1.0 K words
- ◆ Internal RAM size : 49 bytes
(36 general purpose registers, 13 special registers)
- ◆ 37 single word instructions
- ◆ 14-bit instructions
- ◆ 8-level stacks
- ◆ Operating voltage : 2.5 V ~ 6.5 V (PRD Disable)
- ◆ 4.5 V ~ 6.5 V (PRD Enable)
- ◆ Operating frequency : DC ~ 20 MHz
- ◆ The most fast execution time is 200 ns under 20 MHz in all single cycle instructions except the branch instruction
- ◆ Addressing modes include direct, indirect and relative addressing modes
- ◆ Power-on Reset
- ◆ Power edge-detector Reset
- ◆ Power range-detector Reset
- ◆ Sleep Mode for power saving
- ◆ 3 interrupt sources:
 - External INT pin
 - TMR0 timer
 - PortB<7:4> interrupt on change

- ◆ 4 types of oscillator can be selected by programming option:
 - RC - Low cost RC oscillator
 - LFXT - Low frequency crystal oscillator
 - XTAL - Standard crystal oscillator
 - HFXT - High frequency crystal oscillator
- ◆ 8-bit real time clock/counter(RTCC) with 8-bit programmable prescaler
- ◆ On-chip RC oscillator based Watchdog Timer(WDT)
- ◆ 13 I/O pins with their own independent direction control

3. Applications

The application areas of this MDT2060 range from appliance motor control and high speed automotive to low power remote transmitters/receivers, pointing devices, and telecommunications processors, such as Remote controller, small instruments, chargers, toy, automobile and PC peripheral ... etc.

4. Pin Assignment

PA2	1	18	PA1
PA3	2	17	PA0
PA4/RTCC	3	16	OSC1
/MCLR	4	15	OSC2
V _{ss}	5	14	V _{dd}
PB0/INT	6	13	PB7
PB1	7	12	PB6
PB2	8	11	PB5
PB3	9	10	PB4

5. Pin Function Description

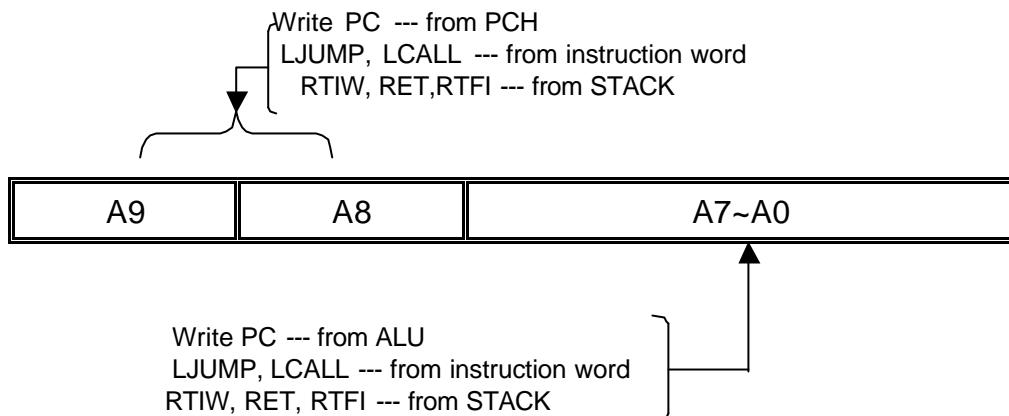
Pin Name	I/O	Function Description
PA0~PA3	I/O	Port A, TTL input level
PB0~PB7	I/O	Port B, TTL input level / PB0:External interrupt input , PB4~PB7:Interrupt on pin change
RTCC/PA4	I/O	Real Time Clock/Counter, Schmitt Trigger input levels Open drain output
/MCLR	I	Master Clear, Schmitt Trigger input levels
OSC1	I	Oscillator Input
OSC2	O	Oscillator Output
V _{dd}		Power supply
V _{ss}		Ground

6. Memory Map

(A) Register Map

Address	Description
BANK0	
00	Indirect Addressing Register
01	RTCC
02	PCL
03	STATUS
04	MSR
05	Port A
06	Port B
0A	PCH
0B	INTS
0C~2F	General purpose register
BANK1	
01	TMR
05	CPIO A
06	CPIO B
07	PSTA

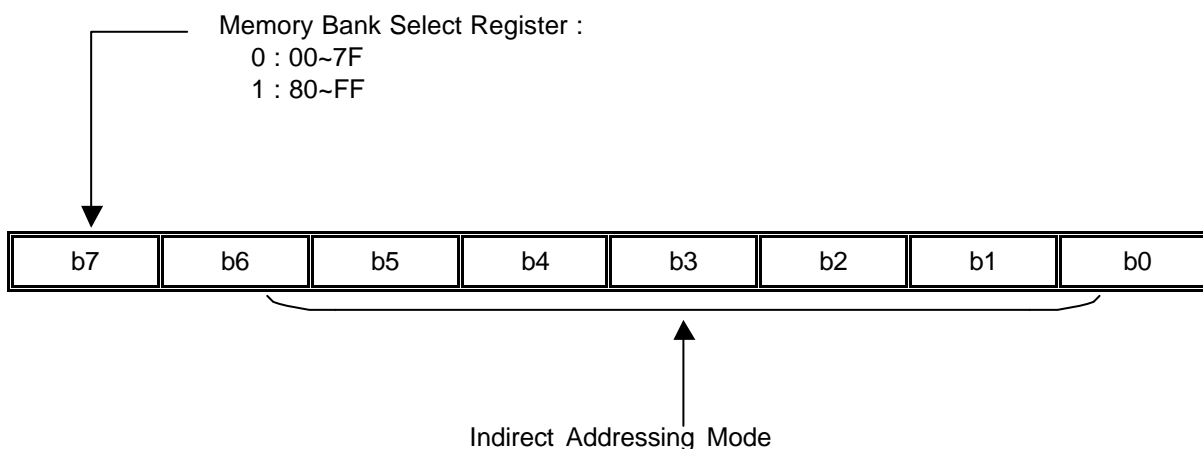
- (1) IAR (Indirect Address Register) : R00
- (2) RTCC (Real Time Counter/Counter Register) : R01
- (3) PC (Program Counter) : R02,R0A



- (4) STATUS (Status register) : R03

Bit	Symbol	Function
0	C	Carry bit
1	HC	Half Carry bit
2	Z	Zero bit
3	PF	Power down Flag bit
4	TF	WDT Timer overflow Flag bit
5	RBS0	Register Bank Select bit : 0 : 00H --- 7FH 1 : 80H --- FFH
7~6	—	General purpose bit

- (5) MSR (Memory Bank Select Register) : R4



(6) PORT A : R05
PA4~PA0, I/O Register

(7) PORT B : R06
PB7~PB0, I/O Register

(8)PCH (High byte of PC) : R0A

Bit	Function
1~0	High byte of PC
7~2	Unimplemented, reads as ' 0 '

(9) INTS (Interrupt Status Register) : R0B

Bit	Symbol	Function
0	RBIF	PORT B change interrupt flag. Set when PB <7:4> inputs change
1	INTF	Set when INT interrupt occurs. INT interrupt flag.
2	TIF	Set when TMR overflows.
3	RBIE	0 : disable PB change interrupt 1 : enable PB change interrupt
4	INTS	0 : disable INT interrupt 1 : enable INT interrupt
5	TIS	0 : disable TMR interrupt 1 : enable TMR interrupt
6	--	Unimplemented
7	GIS	0 : disable global interrupt 1 : enable global interrupt

(10) TMR (Time Mode Register) : R81

Bit	Symbol	Function		
		Prescaler Value	RTCC rate	WDT rate
2—0	PS2—0	0 0 0	1 : 2	1 : 1
		0 0 1	1 : 4	1 : 2
		0 1 0	1 : 8	1 : 4
		0 1 1	1 : 16	1 : 8
		1 0 0	1 : 32	1 : 16
		1 0 1	1 : 64	1 : 32
		1 1 0	1 : 128	1 : 64
		1 1 1	1 : 256	1 : 128

Bit	Symbol	Function
3	PSC	Prescaler assignment bit : 0 — RTCC 1 — Watchdog Timer
4	TCE	RTCC signal Edge : 0 — Increment on low-to-high transition on RTCC pin 1 — Increment on high-to-low transition on RTCC pin
5	TCS	RTCC signal set : 0 — Internal instruction cycle clock 1 — Transition on RTCC pin
6	IES	Interrupt edge select 0 — Interrupt on falling edge on PB0 1 — Interrupt on rising edge on PB0
7	PBPH	PORTB pull-hi 0 — PORTB pull-hi are enable 1 — PORTB pull-hi are disable

(11) CPIO A (Control Port I/O Mode Register) : R85

= "0", I/O pin in output mode;

= "1", I/O pin in input mode.

(12) CPIO B (Control Port I/O Mode Register) : R86

= "0", I/O pin in output mode;

= "1", I/O pin in input mode.

(13) PSTA : R87

Bit	Symbol	Function
0	PRDB	0:Power range-detector Reset occurred 1:No Power range-detector Reset Occurred
1	PORB	0:Power on Reset occurred 1:No Power on Reset occurred

(14) Configurable options for EPROM (Set by writer) :

Oscillator Type
RC Oscillator
HFXT Oscillator
XTAL Oscillator
LFXT Oscillator

Watchdog Timer control
Watchdog timer disable all the time
Watchdog timer enable all the time

Power-range control
Power-range disable
Power-range enable

Oscillator-start Timer control
0ms
80ms

Power-edge Detect
PED Disable
PED Enable

Security state
Security weak Disable
Security Disable
Security Enable

The default security state of EPROM is weak disable. Once the IC was set to enable or disable, it's forbidden to change.

(B) Program Memory

Address	Description
000-3FF	Program memory
000	The starting address of power on, external reset or WDT time-out reset.
004	Interrupt vector

7. Reset Condition for all Registers

Register	Address	Power-On Reset, Power range detector Reset	/MCLR or WDT Reset	Wake-up from SLEEP
IAR	00h	-	-	-
RTCC	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PC	0Ah,02h	00 0000 0000	00 0000 0000	00 0000 0100
STATUS	03h	0001 1xxx	000# #uuu	000# #uuu
MSR	04h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORT A	05h	-- -1 xxxx	-- -1 uuuu	-- -u uuuu
PORT B	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu
INTS	0Bh	0000 0001	0000 000u	uuuu uuuu

Instruction Code	Mnemonic Operands	Function	Operating	Status
011101 trrrrrr	DECR R, t	Decrement register	R - 1 t	Z
011110 trrrrrr	DECRSZ R, t	Decrement register, skip if zero	R - 1 t	None
010010 trrrrrr	ANDWR R, t	AND W and register	R W t	Z
110100 iiiiiii	ANDWI i	AND W and immediate	i W W	Z
010011 trrrrrr	IORWR R, t	Inclu. OR W and register	R W t	Z
110101 iiiiiii	IORWI i	Inclu. OR W and immediate	i W W	Z
010100 trrrrrr	XORWR R, t	Exclu. OR W and register	R W t	Z
110110 iiiiiii	XORWI i	Exclu. OR W and immediate	i W W	Z
011111 trrrrrr	COMR R, t	Complement register	/R t	Z
010110 trrrrrr	RRR R, t	Rotate right register	R(n) R(n-1), C R(7), R(0) C	C
010101 trrrrrr	RLR R, t	Rotate left register	R(n) r(n+1), C R(0), R(7) C	C
010000 1xxxxxxx	CLRW	Clear working register	0 W	Z
010001 0rrrrrr	CLRR R	Clear register	0 R	Z
0000bb brrrrrr	BCR R, b	Bit clear	0 R(b)	None
0010bb brrrrrr	BSR R, b	Bit set	1 R(b)	None
0001bb brrrrrr	BTSC R, b	Bit Test, skip if clear	Skip if R(b)=0	None
0011bb brrrrrr	BTSS R, b	Bit Test, skip if set	Skip if R(b)=1	None
100nnn nnnnnnn	LCALL n	Long CALL subroutine	n PC, PC+1 Stack	None
101nnn nnnnnnn	LJUMP n	Long JUMP to address	n PC	None
110111 iiiiiii	ADDWI i	Add immediate to W	W+i W	C,HC,Z
110001 iiiiiii	RTIW i	Return, place immediate to W	Stack PC,i W	None
111000 iiiiiii	SUBWI i	Subtract W from immediate	i-W W	C,HC,Z
010000 00001001	RTFI	Return from interrupt	Stack PC,1 GIS	None

Note :

W	: Working register	b	: Bit position
WT	: Watchdog timer	t	: Target
TMODE	: TMODE mode register	0	: Working register
CPIO	: Control I/O port register	1	: General register
TF	: Timer overflow flag	R	: General register address
PF	: Power loss flag	C	: Carry flag
PC	: Program Counter	HC	: Half carry
OSC	: Oscillator	Z	: Zero flag
Inclu.	: Inclusive ' '	/	: Complement
Exclu.	: Exclusive ' '	x	: Don't care
AND	: Logic AND ' '	i	: Immediate data (8 bits)
		n	: Immediate address

