

## 1. General Description

This EPROM-Based 8-bit micro-controller uses a fully static CMOS technology process to achieve higher speed and smaller size with the low power consumption and high noise immunity. On chip memory includes 4K words of EPROM, and 192 bytes of static RAM.

## 2. Features

- ◆ RISC CPU
- ◆ Fully static design
- ◆ 37 single word instructions
- ◆ 4K x 14 program memory.
- ◆ 192 bytes RAM for data
- ◆ 35 bi-directional I/O
- ◆ Eight level hardware stacks
- ◆ Watchdog timer with on-chip RC oscillator.
- ◆ Interrupt capability
- ◆ Timer0 : 8-bit timer with 8-bit prescaler
- ◆ Timer1 : 8-bit timer with 8-bit compare register. This timer can be used as carrier generator.
- ◆ Sleep mode for power saving.
- ◆ PB and PD with port change wake-up interrupt.

## 3. Applications

The application areas of this MDT10P65 range from appliance motor control and high speed automotive to low power remote transmitters / receivers and tele-communications processors, such as Remote controller, small instruments, toy, automobile and keyboard ..etc.

## 4. Pin Diagram

PA6	1	42	PA7
/RES	2	41	PB7
PA0	3	40	PB6
PA1	4	39	PB5
PA2	5	38	PB4
PA3	6	37	PB3
PA4/T0CLK	7	36	PB2
PA5	8	35	PB1
PE0	9	34	PB0/IRQ
PE1	10	33	VDD
PE2	11	32	VSS
VDD	12	31	PD7
VSS	13	30	PD6
OSC1	14	29	PD5
OSC2	15	28	PD4
PC0/T1OSCO	16	27	PC7
PC1/T1OSCI	17	26	PC6
PC2	18	25	PC5
PC3	19	24	PC4
PD0	20	23	PD3
PD1	21	22	PD2

## 5. Pin function description

Pin name	Type	Buffer type	Description
OSC1	I		Oscillator input
OSC2	O		Oscillator out
/RES	I	ST	Reset input
PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7	I/O I/O I/O I/O I/O I/O I/O I/O	TTL TTL TTL TTL ST TTL TTL TTL	Bi-directional I/O port A. Port A can be software programmed for internal 100K ohm pull-up on all pins PA0 ~PA3 Output_Lo sink current only 14mA  Can be clock input to Timer0.
PB0/IQR PB1 PB2 PB3 PB4 PB5 PB6 PB7	I/O I/O I/O I/O I/O I/O I/O I/O	ST/TTL TTL TTL TTL TTL TTL TTL TTL	Bi-directional I/O port B. Port B can be software programmed for internal 27K ohm pull-up on all pins. PB0-PB7 can generate interrupt on pin state change. Can be the external interrupt pin.
PC0 PC1 PC2 PC3 PC4 PC5 PC6 PC7	I/O I/O I/O I/O I/O I/O I/O I/O	ST ST ST ST ST ST ST ST	Bi-directional I/O port C. Port C can be software programmed for internal 100K pull-up on all pins. Can be Timer1 oscillator output or Timer1 clock input. Can be Timer1 oscillator input.
PD0-PD7	I/O	ST	Bi-directional port. All pins can generate interrupt on pin state change. Port D can be software programmed for internal 100K pull-up on all pins.
PE0 PE1 PE2	I/O I/O I/O	ST ST ST	Bi-directional port E. Port E can be software programmed for internal 100K pull-up on all pins.
Vdd			Power input
Vss			Ground pin

## 6. Memory Mapping

### 6.1 Program memory :

0000h	Reset Vector
0001h	
0002h	
0003h	
0004h	Peripheral interrupt Vector
0005h	Program memory (Page 0)
07FFh	
0800h	
0FFFh	
	Program memory (Page 1)

### 6.2 Register file map :

	BANK 0	BANK 1		
00h	INDR	INDR	80h	
01h	TMR0	OPTION	81h	
02h	PCL	PCL	82h	
03h	STATUS	STATUS	83h	
04h	MSR	MSR	84h	
05h	PA	PAC	85h	
06h	PB	PBC	86h	
07h	PC	PCC	87h	
08h	PD	PDC	88h	
09h	PE	PEC	89h	
0Ah	PCHLAT	PCHLAT	8Ah	
0Bh	IRQCON	IRQCON	8Bh	
0Ch	PIR1	PIE1	8Ch	
0Dh	PIR2	PIE2	8Dh	
0Eh	TMR1L	PWRCON	8Eh	
0Fh			8Fh	
10h	T1CON	OPTION2	90h	
11h			91h	
12h			92h	
13h			93h	
14h			94h	
15h	CCPR1L		95h	
16h			96h	
17h	CCPR1E		97h	
18h			98h	
1Fh			9Fh	
20h	General Purpose Register	General Purpose Register	A0h	
7Fh				

■ Unimplemented memory location.

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00	Indirect addressing register
01	Timer0 register
02	Program counter low byte
03	Status register
	Bit 0 : Carry
	1 : Digit carry
	2 : Zero flag
	3 : Power-down
	4 : WDT time-out
	5 : Register bank select (For direct addressing)
	=0 Bank 0 (00h-7Fh)
	=1 Bank 1 (80h-FFh)
	7-6 : Always read as zero.
04	Memory select register
05	Port A data register
06	Port B data register
07	Port C data register
08	Port D data register
09	Port E data register
	Bit 2-0 – Port E data register.
	7-3 – Unimplemented. Always set as 0.
0A	Program memory segment register
0B	Interrupt control register
	Bit 0 – PB port change interrupt flag bit.
	1 – PB0/IRQ external interrupt flag bit.
	2 – Timer0 overflow interrupt flag bit.
	3 – PB port change interrupt enable bit.
	4 – PB0/IRQ external interrupt enable bit.
	5 – Timer0 overflow interrupt enable bit.
	6 – Peripheral interrupt enable bit.
	7 – Global interrupt enable bit.
0C	Peripheral interrupt flag register 1.
	Bit 0 – Timer1 overflow interrupt flag bit
	7-1 – Unimplemented. Always read as 0.
0D	Peripheral interrupt flag register 2.
	Bit 6-0 – Unimplemented. Read as zero.
	7 – PD port change interrupt flag bit
0E	Timer1 data register low byte.
0F	Unimplemented..

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- 10 Timer1 control register  
Bit 0 – Timer1 enable bit  
1 – Timer1 clock source select  
2 – Timer 1 external clock synchronization control bit  
3 – Timer 1 oscillator enable control bit  
5-4 – Timer 1 prescaler select bits  
7-6 – Unimplemented. Always read as 0.
- 11-14 Unimplemented.
- 15 Timer1 compare register
- 16 Unimplemented.
- 17 Timer1 compare control register  
Bit 7-1 –Unimplemented. Always set as 0.  
0 – compare enable bit
- 18-1F Unimplemented.
- 20-7F General purpose register
- 80 Same as register 00.
- 81 Option register  
Bit 2-0 – Prescaler rate select bits  
3 – Prescaler assign bit  
4 – Timer 0 edge select bit  
5 – Timer 0 clock source select bit  
6 – PB0/IRQ interrupt edge select bit  
7 – Port B pull-up enable bit.
- 82-84 Same as 02H-04H.
- 85 Port A data direction register.
- 86 Port B data direction register.
- 87 Port C data direction register.
- 88 Port D data direction register.
- 89 Port E data direction register.  
Bit 2-0 – Port E data direction register.  
7-3 – Unimplemented. Always set as 0.
- 8A -8B Same as 0AH-0BH.
- 8C Peripheral interrupt control register 1.  
Bit 0 – Timer1 overflow interrupt enable bit.  
7-1 – Unimplemented. Always set these bits to 0.
- 8D Peripheral interrupt control register 2  
Bit 6-0 – Unimplemented.  
7 – PD port change interrupt enable bit.
- 8E Power control register.
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- Bit 0 – Unimplemented. Always read as 0.
- 1 – Power-on reset status bit.
- 7-2 – Unimplemented. Always read as 0.
- 8F Unimplemented.
- 90 Option register 2. ( “ 0 ” Enable ; “ 1 ” Disable )
  - Bit 0-3 – Unimplemented.
  - 4 – PA port pull-up enable bit.
  - 5 – PC port pull-up enable bit.
  - 6 – PD port pull-up enable bit.
  - 7 – PE port pull-up enable bit.
- 91-9F Unimplemented.
- A0-FF General purpose register.

## 7.Reset Condition for all Registers

Register	Address	Power-On Reset, Power range detector Reset	/MCLR or WDT Reset	Wake-up from SLEEP
IAR	00h(80h)	0000 0000	0000 0000	uuuu uuuu
RTCC	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h(82h)	0000 0000	0000 0000	0000 0100
STATUS	03h(83h)	0001 1xxx	000# #uuu	000# #uuu
MSR	04h(84h)	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORT A	05h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORT B	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORT C	07h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORT D	08h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORT E	09h	---- -xxx	---- -uuu	---- -uuu
PCHLAT	0Ah(8Ah)	---- 0000	---- 0000	---- uuuu
IRQCON	0Bh(8Bh)	0000 0001	0000 0001	uuuu uuuu
PIR1	0Ch	---- -x	---- -u	---- -u
PIR2	0Dh	1--- ----	1--- ----	u--- ----
TMR1L	0Eh	xxxx xxxx	Uuuu uuuu	Uuuu uuuu
T1CON	10h	--00 0000	--00 0000	--uu uuuu
CCPR1L	15h	Xxxx xxxx	uuuu uuuu	--uu uuuu
CCPR1E	17h	---- -0	---- -0	---- -u
OPTION	81h	1111 1111	1111 1111	uuuu uuuu
CPIOA	85h	1111 1111	1111 1111	uuuu uuuu
CPIOB	86h	1111 1111	1111 1111	uuuu uuuu
CPIOC	87h	1111 1111	1111 1111	uuuu uuuu
CPIOD	88h	1111 1111	1111 1111	uuuu uuuu
CPIOE	89h	---- -111	---- -111	---- -uuu
PIE1	8Ch	---- -0	---- -0	---- -u
PIE2	8Dh	0--- ----	0--- ----	u--- ----
PWRCON	8Eh	---- #-	---- -u-	---- -u-
OPTION2	90h	1111 ----	1111 ----	uuuu ----

Note : u = unchanged , x = unknown , - = unimplemented , read as "0"

# = value depends on the condition of the following table

Condition	Status bit 4	Status bit 3	PWRCON bit 1
POWR ON RESET	1	1	0
/MCLR reset (not during SLEEP)	u	u	u
/MCLR reset during SLEEP	1	0	u
WDT reset (not during SLEEP)	0	1	u
WDT reset during SLEEP	0	0	u
Interrupt Wake-up during SLEEP	1	0	u

## 8. Instruction Set

Instruction Code	Mnemonic Operands	Function	Operation	Status
010000 00000000	NOP	No operation	None	
010000 00000001	CLRWT	Clear Watchdog timer	0 WT	TF, PF
010000 00000010	SLEEP	Sleep mode	0 WT, stop OSC	TF, PF
010000 00000011	TMODE	Load W to TMODE register	W TMODE	None
010000 00000rrr	CPIO R	Control I/O port register	W CPIO r	None
010001 1rrrrrrr	STWR R	Store W to register	W R	None
011000 trrrrrrr	LDR R, t	Load register	R t	Z
111010 iiiiii	LDWI I	Load immediate to W	I W	None
010111 trrrrrrr	SWAPR R, t	Swap halves register	[R(0~3) ↔ R(4~7)] t	None
011001 trrrrrrr	INCR R, t	Increment register	R + 1 t	Z
011010 trrrrrrr	INCRSZ R, t	Increment register, skip if zero	R + 1 t	None
011011 trrrrrrr	ADDWR R, t	Add W and register	W + R t	C, HC, Z
011100 trrrrrrr	SUBWR R, t	Subtract W from register	R - W t (R+W+1 t)	C, HC, Z
011101 trrrrrrr	DECR R, t	Decrement register	R - 1 t	Z
011110 trrrrrrr	DECRSZ R, t	Decrement register, skip if zero	R - 1 t	None
010010 trrrrrrr	ANDWR R, t	AND W and register	R W t	Z
110100 iiiiii	ANDWI i	AND W and immediate	i W W	Z
010011 trrrrrrr	IORWR R, t	Inclu. OR W and register	R W t	Z
110101 iiiiii	IORWI i	Inclu. OR W and immediate	i W W	Z
010100 trrrrrrr	XORWR R, t	Exclu. OR W and register	R W t	Z

Instruction Code	Mnemonic Operands	Function	Operation	Status
110110 iiiiii	XORWI i	Exclu. OR W and immediate	i W W	Z
011111 trrrrrr	COMR R, t	Complement register	/R t	Z
010110 trrrrrr	RRR R, t	Rotate right register	R(n) R(n-1),C R(7), R(0) C	C
010101 trrrrrr	RLR R, t	Rotate left register	R(n) r(n+1), C R(0)R(7) C	C
010000 1xxxxxx	CLRW	Clear working register	0 W	Z
010001 0rrrrrr	CLRR R	Clear register	0 R	Z
0000bb brrrrrr	BCR R, b	Bit clear	0 R(b)	None
0010bb brrrrrr	BSR R, b	Bit set	1 R(b)	None
0001bb brrrrrr	BTSC R, b	Bit Test, skip if clear	Skip if R(b)=0	None
0011bb brrrrrr	BTSS R, b	Bit Test, skip if set	Skip if R(b)=1	None
100nnn nnnnnnn	LCALL n	Long CALL subroutine	n PC, PC+1 Stack	None
101nnn nnnnnnn	LJUMP n	Long JUMP to address	n PC	None
110001 iiiiii	RTIW i	Return,place immediate to W	Stack PC,i W	None
110111 iiiiii	ADDWI	Add immediate to W	W+i W	C,HC,Z
111000 iiiiii	SUBWI	Subtract W from immediate	i-W W	C,HC,Z
010000 00001001	RTFI	Return from interrupt	Stack PC, 1 GIS	None
010000 00000100	RET	Return from subroutine	Stack PC	None

Note :

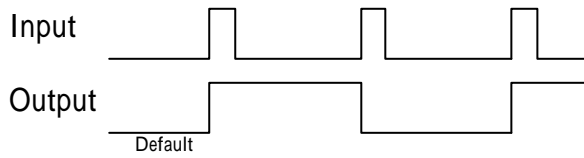
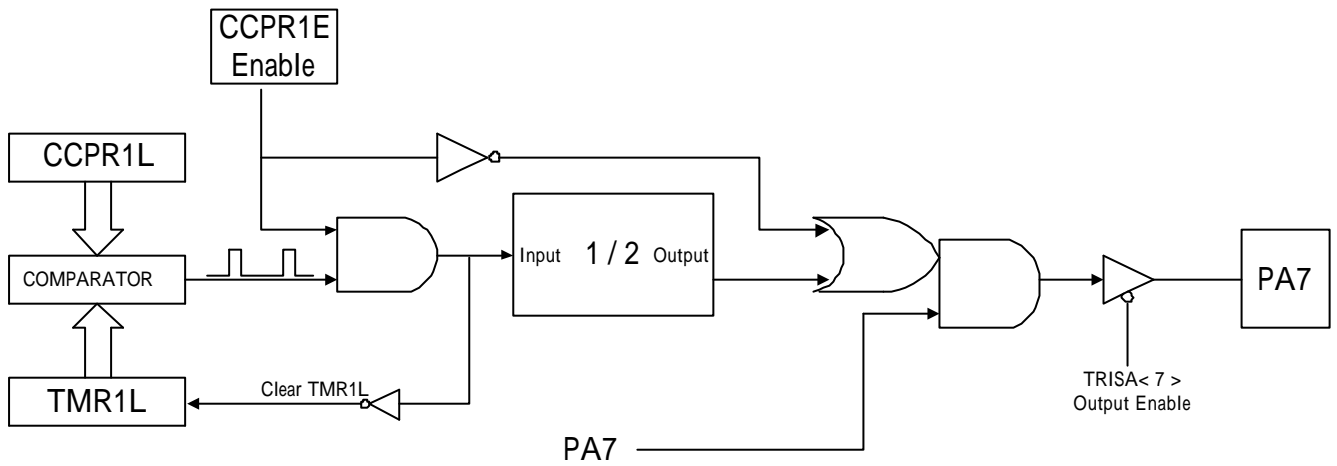
W	: Working register	b	: Bit position
WT	: Watchdog timer	t	: Target
TMODE	: TMODE mode register	0	: Working register
CPIO	: Control I/O port register (PA , PB , PC Only)	1	: General register
TF	: Timer overflow flag	R	: General register address
PF	: Power loss flag	C	: Carry flag
PC	: Program Counter	HC	: Half carry
OSC	: Oscillator	Z	: Zero flag
Inclu.	: Inclusive ‘ ’	/	: Complement
Exclu.	: Exclusive ‘ ’	x	: Don’ t care
AND	: Logic AND ‘ ’	i	: Immediate data ( 8 bits )
		n	: Immediate address

**9. NOTE**

**9-1. Port Pull\_up resister**

PA Pull\_up PA0 ~ 4= 50K ; PA5= 100K ; PA6 ~ 7= 50K  
 PB Pull\_up = 27K  
 PC Pull\_up = 100K  
 PD Pull\_up = 100K  
 PE Pull\_up = 100K

**9-2. Timer1 CCP Mode**



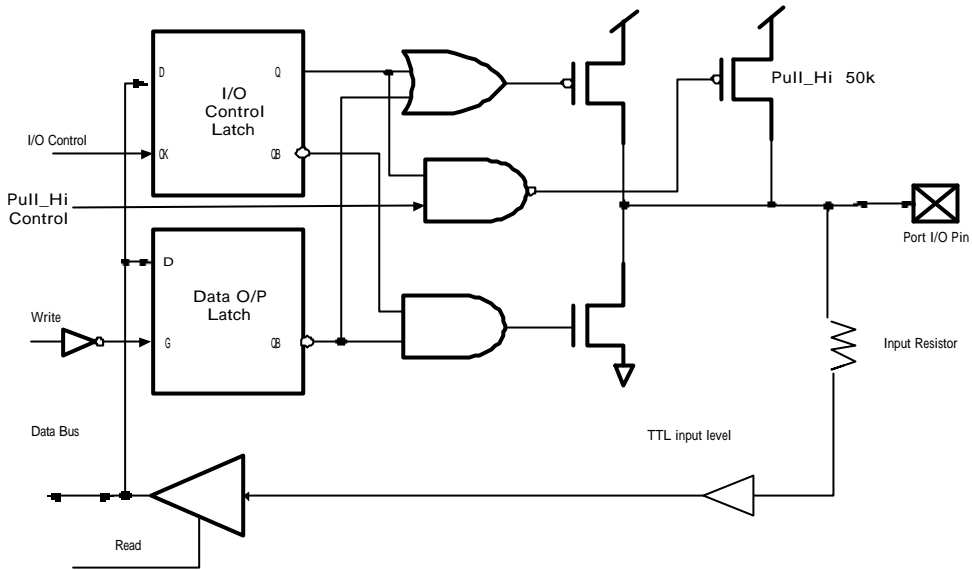
## 10. Electrical Characteristics

(Operating temperature at 25 °C).

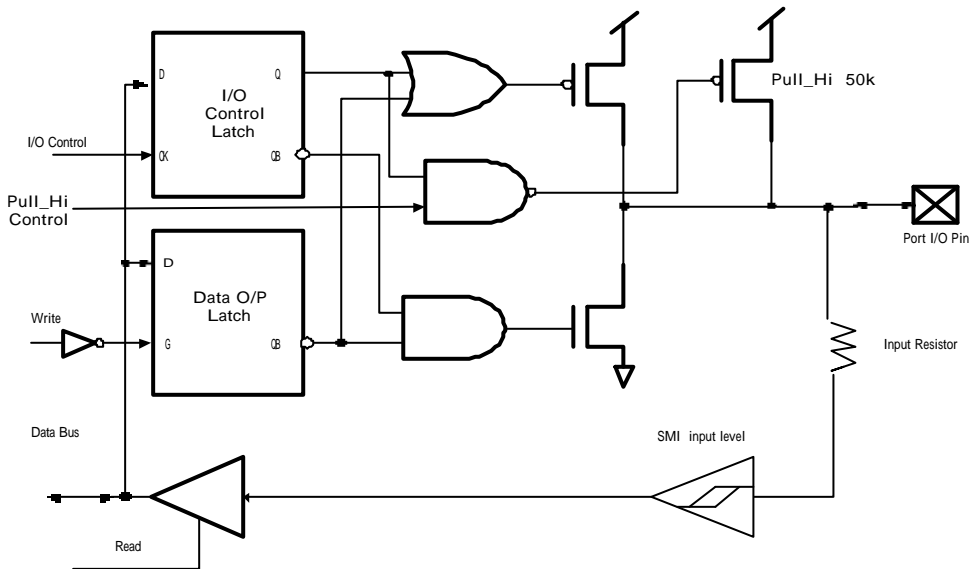
Sym	Description	Condition	Min	Typ	Max	Unit
V <sub>DD</sub>	Operating voltage		2.3		6.3	V
V <sub>IL</sub>	Input Low Voltage PA, PB	V <sub>DD</sub> =5V	-0.6		1.0	V
		PC, PD, PE, /MCLR	V <sub>DD</sub> =5V	-0.6	1.0	V
V <sub>IH</sub>	Input high Voltage PA, PB	V <sub>DD</sub> =5V	2.0		V <sub>DD</sub>	V
		PC, PD, PE, RTCC, /MCLR	V <sub>DD</sub> =5V	3.2	V <sub>DD</sub>	V
I <sub>IL</sub>	Input leakage current	V <sub>DD</sub> =5V			+/-1	μA
V <sub>OL</sub>	Output Low Voltage PA, PB, PC, PD, PE	V <sub>DD</sub> =5V, I <sub>OL</sub> =20mA		0.4		V
		V <sub>DD</sub> =5V, I <sub>OL</sub> =5mA		0.1		V
V <sub>OH</sub>	Output High Voltage PA, PB, PC, PD, PE	V <sub>DD</sub> =5V, I <sub>OH</sub> = -20mA		3.8		V
		V <sub>DD</sub> =5V, I <sub>OH</sub> = -5mA		4.5		V
I <sub>slp</sub>	Sleep current (WDT disable)	V <sub>DD</sub> = 2.3 ~ 6.3 V		0.1	1.0	μA
I <sub>slp</sub>	Sleep current (WDT enable)	V <sub>DD</sub> = 2.3 V		0.1		μA
		V <sub>DD</sub> = 3.0 V		3		μA
		V <sub>DD</sub> = 4.0 V		8		μA
		V <sub>DD</sub> = 5.0 V		16		μA
		V <sub>DD</sub> = 6.3 V		35		μA
V <sub>PR</sub>	Power Edge-detector Reset Voltage		1.1		1.3	V
T <sub>wdt</sub>	The basic WDT time-out cycle time	V <sub>DD</sub> = 2.3 V		26.4		mS
		V <sub>DD</sub> = 3.0 V		22.7		mS
		V <sub>DD</sub> = 4.0 V		20.1		mS
		V <sub>DD</sub> = 5.0 V		18.1		mS
		V <sub>DD</sub> = 6.3 V		16.4		mS
T <sub>FLT</sub>	/MCLR filter	V <sub>DD</sub> = 5.0 V		600		nS

11. Port A Equivalent Circuit

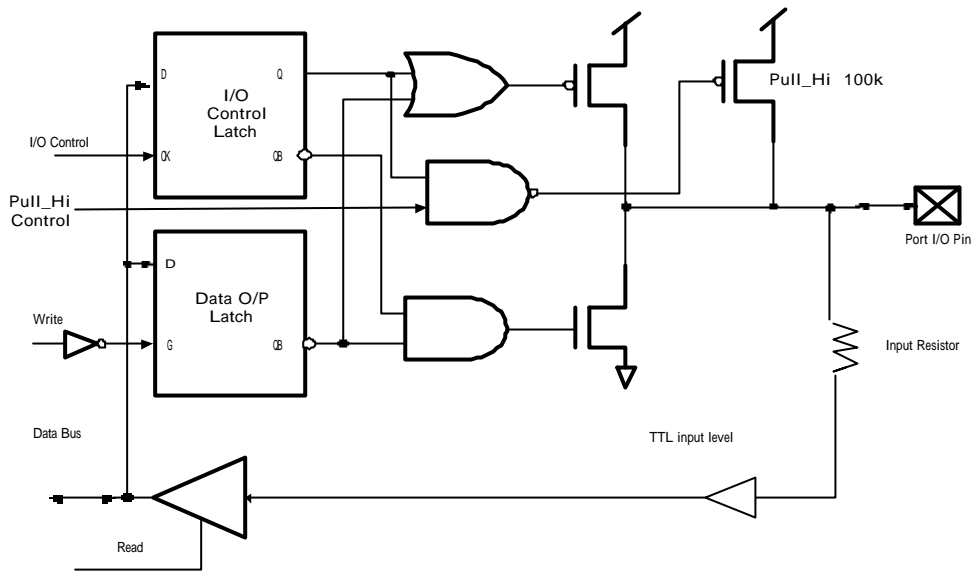
PA0-PA3 & PA6-PA7



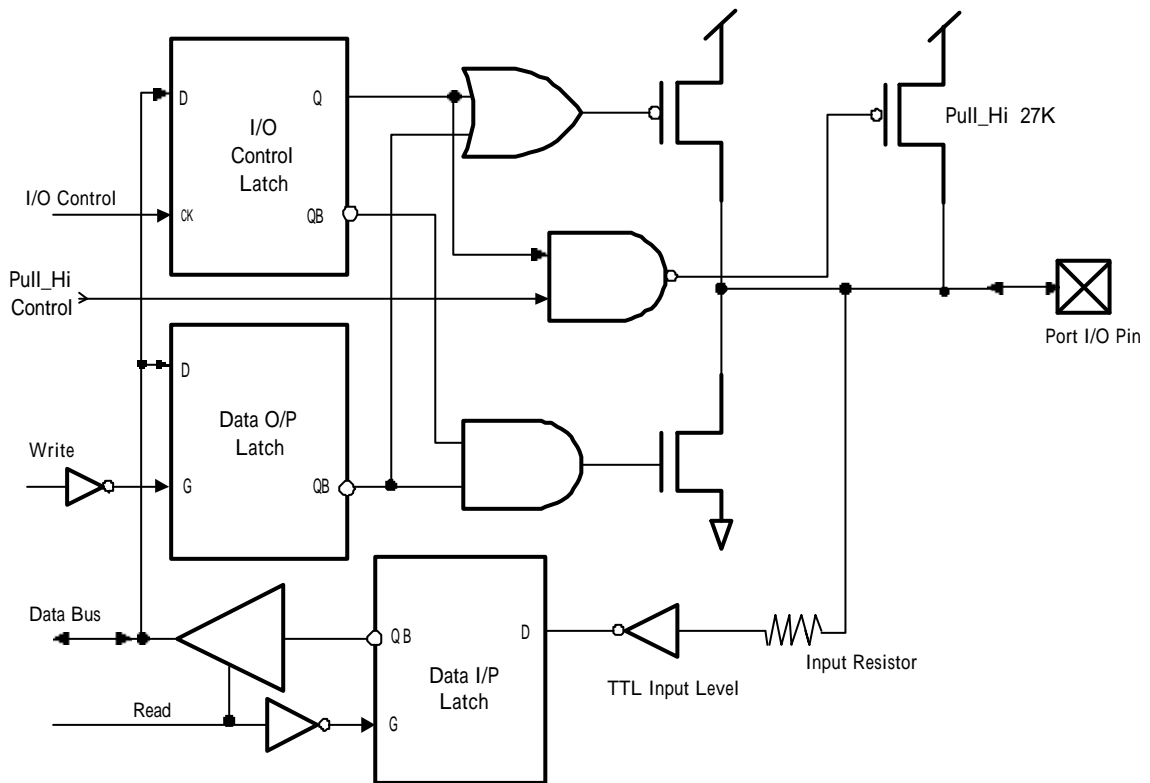
PA4



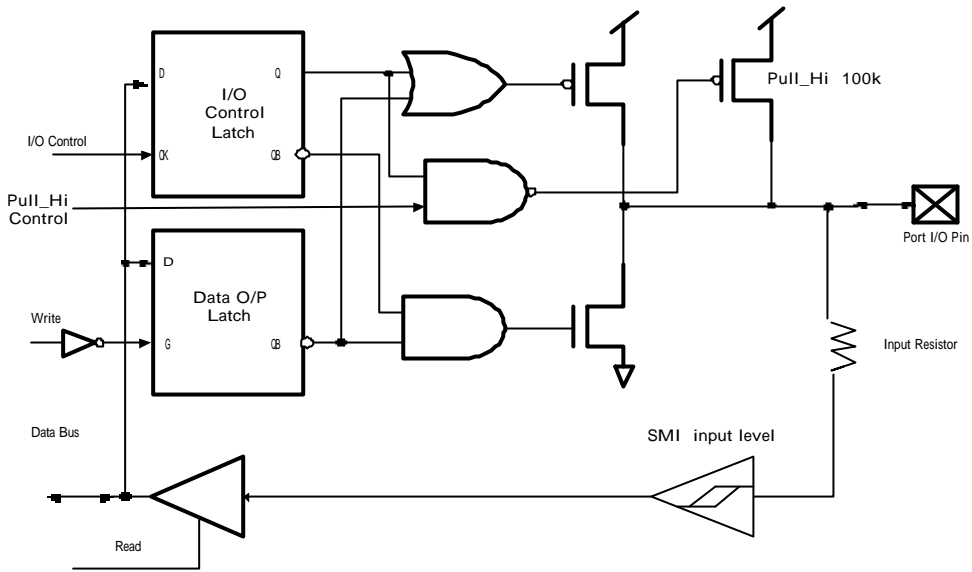
PA5



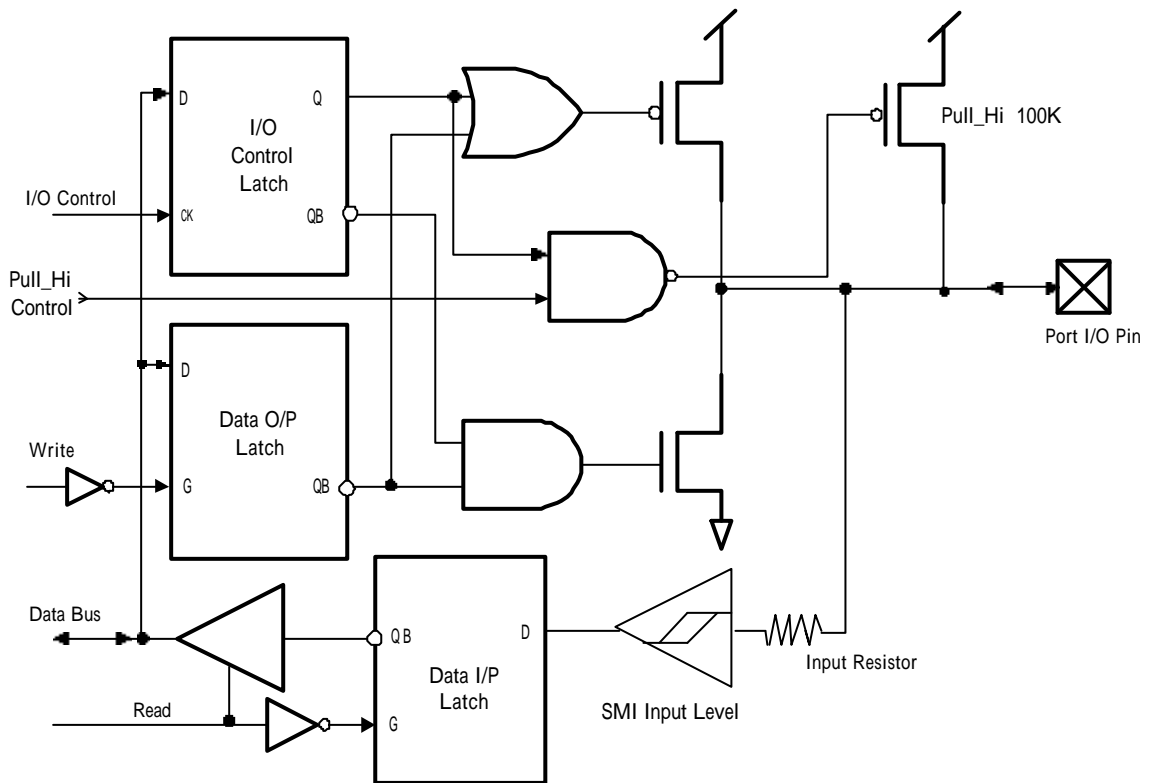
**Port B Equivalent Circuit**



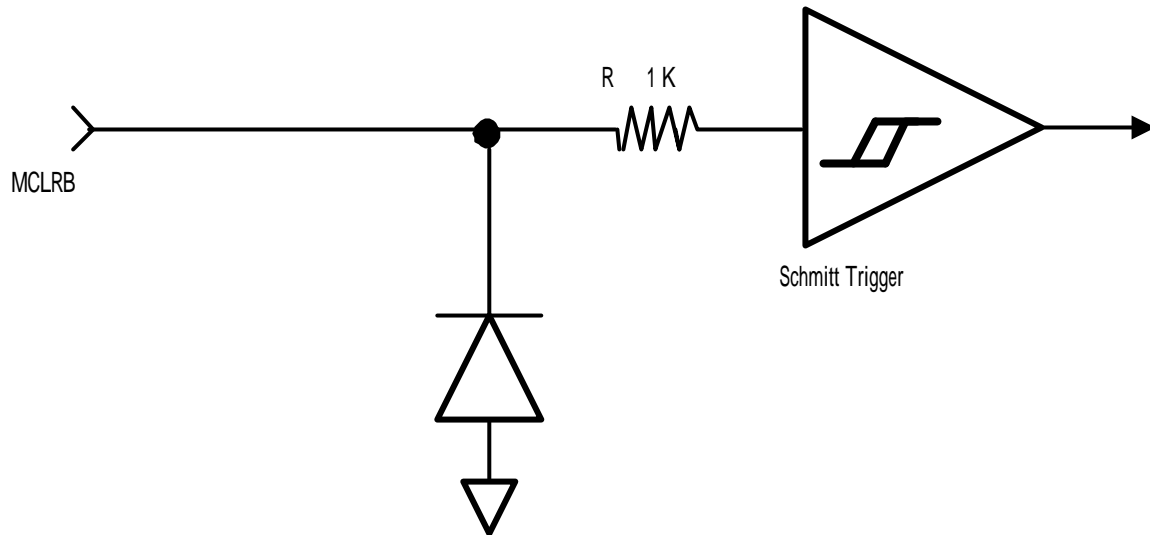
**Port C & Port E Equivalent Circuit**



**Port D Equivalent Circuit**



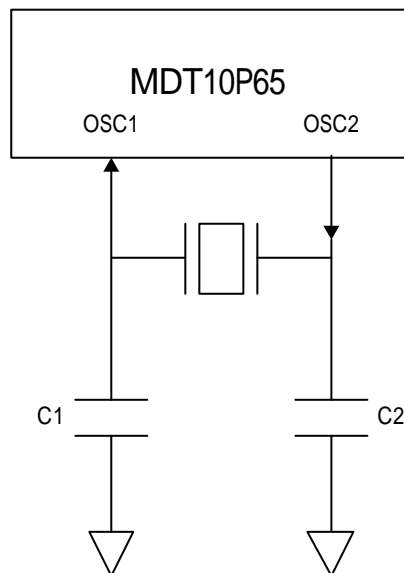
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**12. MCLRB Input Equivalent Circuit**

**13. External Capacitor Selection For Crystal Oscillator**

@  $V_{dd} = 5.0\text{ V}$

Osc. Type	Resonator Freq.	Capacity Range
HF	20 MHz	10 pF ~ 50 pF
	10 MHz	20 pF ~ 50 pF
	4 MHz	10 pF ~ 30 pF
XT	10 MHz	10 pF ~ 50 pF
	4 MHz	10 pF ~ 50 pF
	1 MHz	20 pF ~ 50 pF
LF	1 MHz	20 pF ~ 30 pF
	455 K	20 pF ~ 30 pF
	32 K	20 pF ~ 50 pF



To increase the stability of oscillator and the ability of anti-noise, the above values of the external capacitor are for reference only, but the higher capacitance also increases the start-up time.