

1. General Description

This EPROM-Based 8bit micro-controller uses a fully static CMOS technology process to achieve higher speed and smaller size with the low power consumption and high noise immunity. On chip memory includes 1K words of ROM, and 72 bytes of static RAM.

2. Features

The followings are some of the features on the hardware and software :

- ◆ Fully COMS static design
- ◆ 8-bit data bus
- ◆ On chip EPROM size : 1K words
- ◆ Internal RAM size : 72 bytes
- ◆ 36 single word instructions
- ◆ 14-bit instructions
- ◆ 2-level stacks
- ◆ Operating voltage : 2.5 V ~ 6.0 V
- ◆ Operating frequency : 0 ~ 20 MHz
- ◆ The most fast execution time is 200 ns under 20 MHz in all single cycle instructions except the branch instruction
- ◆ Addressing modes include direct, indirect and relative addressing modes
- ◆ Power-on Reset
- ◆ Sleep Mode for power saving
- ◆ 5 types of oscillator can be selected by programming option:
 - INTRC - Internal 4 MHz RC oscillator
 - RC - Low cost RC oscillator
 - LFXT - Low frequency crystal oscillator
 - XTAL - Standard crystal oscillator
 - HFXT - High frequency crystal oscillator
- ◆ 3 oscillator start-up time can be selected by programming option:
 - 20 ms, 40 ms, 80 ms
- ◆ 8-bit real time clock/counter(RTCC) with 8-bit programmable prescaler
- ◆ On-chip RC oscillator based Watchdog Timer(WDT)
- ◆ Wake-up from sleep on pin change

3. Applications

The application areas of this MDT10P55 range from appliance motor control and high speed automotive to low power remote transmitters/receivers, small instruments, chargers, toy, automobile and PC peripheral ... etc.

4. Pin Assignment

MDT10P55A1P/MDT10P55A1S

VDD	1	14	VSS
PB5	2	13	PB0
PB4	3	12	PB1
PB3	4	11	PB2
PC5/RTCC	5	10	PC0
PC4	6	9	PC1
PC3	7	8	PC2

MDT10P55A3P/MDT10P55A3S

VDD	1	14	VSS
PB5	2	13	PB0
PB4	3	12	PB1
/MCLR	4	11	PB2
PC5/RTCC	5	10	PC0
PC4	6	9	PC1
PC3	7	8	PC2

MDT10P55A2P/MDT10P55A2S

VDD	1	14	VSS
OSC1	2	12	PB0
OSC2/PB4	3	12	PB1
PB3	4	11	PB2
PC5/RTCC	5	10	PC0
PC4	6	9	PC1
PC3	7	8	PC2

MDT10P55A4P/MDT10P55A4S

VDD	1	14	VSS
OSC1	2	13	PB0
OSC2/PB4	3	12	PB1
/MCLR	4	11	PB2
PC5/RTCC	5	10	PC0
PC4	6	9	PC1
PC3	7	8	PC2

5. Pin Function Description

Pin Name	I/O	Function Description
PB5~0	I/O	Port B, TTL input level , PB3 input only.
PC4~0	I/O	Port C, TTL input level
PC5/RTCC	I/O	Real Time Clock/Counter, Schmitt Trigger input levels
/MCLR	I	Master Clear, Schmitt Trigger input levels
OSC1	I	Oscillator Input
OSC2	O	Oscillator Output
V _{dd}		Power supply
V _{ss}		Ground

6. Memory Map

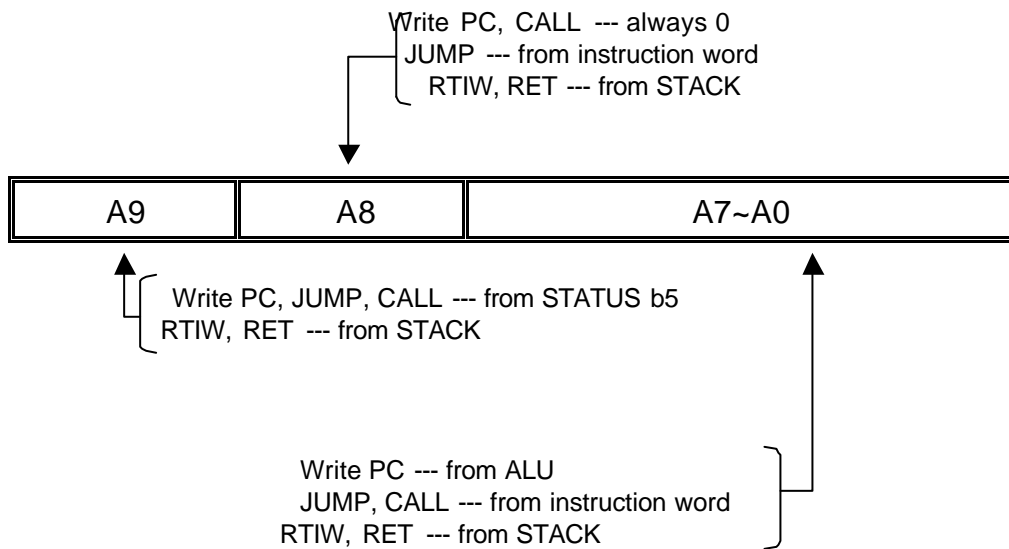
(A) Register Map

Address	Description
00	Indirect Addressing Register
01	RTCC
02	PC
03	STATUS
04	MSR
06	Port B
07	Port C
08~1F 30~3F 50~5F 70~7F	General purpose registers

(1) IAR (Indirect Address Register) : R0

(2) RTCC (Real Time Counter/Counter Register) : R1

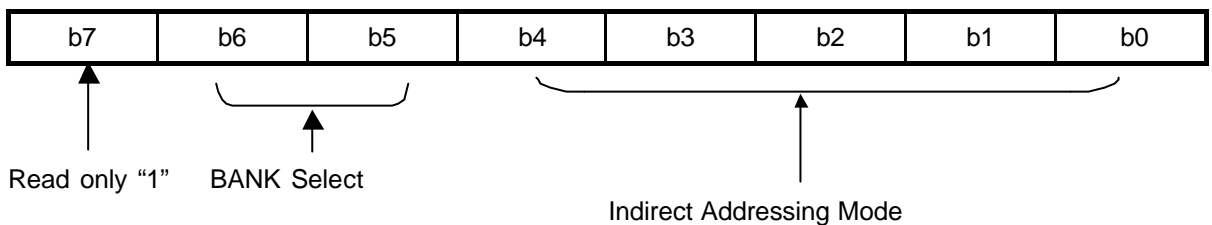
(3) PC (Program Counter) : R2



(4) STATUS (Status register) : R3

Bit	Symbol	Function
0	C	Carry bit
1	HC	Half Carry bit
2	Z	Zero bit
3	PF	Power down bit
4	TF	WDT Timer overflow Flag bit
5	PAGE	ROM page select bit
6	—	Unimplemented
7	PCWUF	Pin change wake up from sleep

(5) MSR (Memory Bank Select Register) : R4



(6) PORT B : R6

PB5~PB0, I/O Register , PB3 input only.

(7) PORT C: R7

PC5~PC0, I/O Register

(8) TMR (Time Mode Register)

Bit	Symbol	Function		
		Prescaler Value	RTCC rate	WDT rate
2—0	PS2—0	0 0 0	1 : 2	1 : 1
		0 0 1	1 : 4	1 : 2
		0 1 0	1 : 8	1 : 4
		0 1 1	1 : 16	1 : 8
		1 0 0	1 : 32	1 : 16
		1 0 1	1 : 64	1 : 32
		1 1 0	1 : 128	1 : 64
		1 1 1	1 : 256	1 : 128
3	PSC	Prescaler assignment bit : 0 — RTCC 1 — Watchdog Timer		

Bit	Symbol	Function
4	TCE	RTCC signal Edge : 0 — Increment on low-to-high transition on RTCC pin 1 — Increment on high-to-low transition on RTCC pin
5	TCS	RTCC signal set : 0 — Internal instruction cycle clock 1 — Transition on RTCC pin
6	PBPHB	PortB pull-high : 0 — Enable 1 — Disable
7	PBWUB	PortB wake-up : 0 — Enable 1 — Disable

(9) CPIO B , CPIO C (Control Port I/O Mode Register)

The CPIO register is “write-only”
= “0”, I/O pin in output mode;
= “1”, I/O pin in input mode.

(10) Configurable options for EPROM (Set by writer) :

Oscillator Type	Oscillator Start-up Time
INTRC Oscillator	20ms,40ms,80ms
RC Oscillator	20ms,40ms,80ms
HFXT Oscillator	20 ms,40ms,80ms
XTAL Oscillator	20ms,40 ms,80ms
LFXT Oscillator	20ms,40 ms,80 ms

Watchdog Timer control
Watchdog timer disable all the time
Watchdog timer enable all the time

Security state
Security weak Disable
Security Disable
Security Enable

The default security state of EPROM is weak disable. Once the IC was set to enable or disable, it's forbidden to change.

(B) Program Memory

Address	Description
000-3FF	Program memory
000	The starting address of power on, external reset or WDT time-out reset.

8. Reset Condition for all Registers

Register	Address	Power-On Reset	/MCLR Reset	WDT Reset
IAR	00h	xxxx xxxx	uuuu uuuu	uuuu uuuu
RTCC	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PC	02h	0000 0000	0000 0000	0000 0000
STATUS	03h	0001 1xxx	#00# #uuu	#00# #uuu
MSR	04h	110x xxxx	110u uuuu	11uu uuuu
PORT B	06h	--xx xxxx	--uu uuuu	--uu uuuu
PORT C	07h	--xx xxxx	--uu uuuu	--uu uuuu

Note : u = unchanged, x = unknown, - = unimplemented, read as "0"

= value depends on the condition of the following table

Condition	Status: bit 7	Status: bit 4	Status: bit 3
/MCLR reset (not during SLEEP)	0	u	u
/MCLR reset during SLEEP	0	1	0
WDT reset (not during SLEEP)	0	0	1
WDT reset during SLEEP	0	0	0
Wake-up from SLEEP on pin change	1	1	0

9. Instruction Set :

Instruction Code	Mnemonic Operands	Function	Operating	Status
010000 00000000	NOP	No operation	None	
010000 00000001	CLRWT	Clear Watchdog timer	0 WT	TF, PF
010000 00000010	SLEEP	Sleep mode	0 WT, stop OSC	TF, PF
010000 00000011	TMODE	Load W to TMODE register	W TMODE	None
010000 00000100	RET	Return	Stack PC	None
010000 00000rrr	CPIO R	Control I/O port register	W CPIO r	None

Instruction Code	Mnemonic Operands	Function	Operating	Status
010001 1rrrrrrr	STWR R	Store W to register	W R	None
011000 trrrrrrr	LDR R, t	Load register	R t	Z
111010 iiiiii	LDWI I	Load immediate to W	I W	None
010111 trrrrrrr	SWAPR R, t	Swap halves register	[R(0-3) ↔ R(4-7)] t	None
011001 trrrrrrr	INCR R, t	Increment register	R + 1 t	Z
011010 trrrrrrr	INCRSZ R, t	Increment register, skip if zero	R + 1 t	None
011011 trrrrrrr	ADDWR R, t	Add W and register	W + R t	C, HC, Z
011100 trrrrrrr	SUBWR R, t	Subtract W from register	R - W t or (R+/W+1 t)	C, HC, Z
011101 trrrrrrr	DECR R, t	Decrement register	R - 1 t	Z
011110 trrrrrrr	DECRSZ R, t	Decrement register, skip if zero	R - 1 t	None
010010 trrrrrrr	ANDWR R, t	AND W and register	R W t	Z
110100 iiiiii	ANDWI i	AND W and immediate	i W W	Z
010011 trrrrrrr	IORWR R, t	Inclu. OR W and register	R W t	Z
110101 iiiiii	IORWI i	Inclu. OR W and immediate	i W W	Z
010100 trrrrrrr	XORWR R, t	Exclu. OR W and register	R W t	Z
110110 iiiiii	XORWI i	Exclu. OR W and immediate	i W W	Z
011111 trrrrrrr	COMR R, t	Complement register	/R t	Z
010110 trrrrrrr	RRR R, t	Rotate right register	R(n) R(n-1), C R(7), R(0) C	C
010101 trrrrrrr	RLR R, t	Rotate left register	R(n) r(n+1), C R(0), R(7) C	C
010000 1xxxxxxx	CLRW	Clear working register	0 W	Z
010001 0rrrrrrr	CLRR R	Clear register	0 R	Z
0000bb brrrrrrr	BCR R, b	Bit clear	0 R(b)	None
0010bb brrrrrrr	BSR R, b	Bit set	1 R(b)	None
0001bb brrrrrrr	BTSC R, b	Bit Test, skip if clear	Skip if R(b)=0	None
0011bb brrrrrrr	BTSS R, b	Bit Test, skip if set	Skip if R(b)=1	None
1000nn nnnnnnnn	LCALL n	Long CALL subroutine	n PC, PC+1 Stack	None
1010nn nnnnnnnn	LJUMP n	Long JUMP to address	n PC	None
110000 nnnnnnnn	CALL n	Call subroutine	n PC, PC+1 Stack	None
110001 iiiiii	RTIW i	Return, place immediate to W	Stack PC,i W	None
11001n nnnnnnnn	JUMP n	JUMP to address	n PC	None

Note :

- | | | | | | |
|--------|---|---------------------------|----|---|---------------------------|
| W | : | Working register | b | : | Bit position |
| WT | : | Watchdog timer | t | : | Target |
| TMODE | : | TMODE mode register | 0 | : | Working register |
| CPIO | : | Control I/O port register | 1 | : | General register |
| TF | : | Timer overflow flag | R | : | General register address |
| PF | : | Power loss flag | C | : | Carry flag |
| PC | : | Program Counter | HC | : | Half carry |
| OSC | : | Oscillator | Z | : | Zero flag |
| Inclu. | : | Inclusive ' ' | / | : | Complement |
| Exclu. | : | Exclusive ' ' | x | : | Don't care |
| AND | : | Logic AND ' ' | i | : | Immediate data (8 bits) |
| | | | n | : | Immediate address |

10. Oscillator start up timer condition :

Oscillator Type	Power-on reset	Subsequent resets
INTRC,RC	20ms,40ms,80ms	300us
HF,XT,LF	20ms,40ms,80ms	20ms,40ms,80ms